Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently Amended) A method according to Claim 30 ~~5~~, wherein the first register includes a block selector for selectively characterizing at least one of such blocks of registers as an indicated block of registers.

3. (Currently Amended) A method according to Claim 30 ~~5~~, wherein the second register includes an operational code.

4. (Original) A method according to Claim 3, wherein the second register includes a port indicator.

5. (Currently Amended) ~~A method for expanding addressing capability of a plurality of registers connected to an interface comprising:~~

~~designating at least two of the plurality of registers as a block of registers;~~

~~providing a plurality of such blocks of registers;~~

~~designating a first register within the plurality of registers that is separate from the blocks of registers for selectively characterizing at least one of such blocks of registers as an indicated block of registers,~~ A method according to Claim 30, wherein said first register comprises a pointer to a plurality of location registers, each of the plurality of location registers indicating at least one such blocks of registers; and

~~designating a second register within the plurality of registers that is separate from the blocks of registers for specifying at least one operation for the indicated block of registers,~~ wherein said second register comprises a pointer to a plurality of control registers, each of the plurality of control registers comprising an operational code; and

wherein said plurality of location registers are associated with said plurality of control

registers such that a first operational code is associated with a first of such blocks of registers and a second operational code is associated with a second of such blocks of registers.

6. (Currently Amended) A method according to Claim 30 ~~5~~, wherein said location and control registers comprise registers compatible with IEEE standard 802.3 clause 22.

7. (Canceled)

8. (Currently Amended) A system according to Claim 31 ~~20~~, wherein ~~each of~~ the ~~respective~~ operational code[[s]] specifies an operation to be performed on the specified block of registers.

9. (Original) A system according to Claim 8, wherein the operation is restricting the specified block of registers to read operations only.

10. (Currently Amended) A system according to Claim 31 ~~20~~, wherein the ~~respective~~ operational code[[s]] specify~~ies~~ control sequencing information.

11. (Original) A system according to Claim 10, wherein the control sequencing information instructs the control engine to proceed to a next block after completing operations with the specified block.

12. (Currently Amended) A system according to Claim 31 ~~20~~, wherein said location register includes a block selector indicating said block.

13. (Currently Amended) A system according to Claim 31 ~~20~~, wherein said location register includes a pointer to a block selector.

14-15. (Canceled)

16. (Currently Amended) A system according to Claim 33~~20~~, wherein said control register is further operable to store a register indicator indicative of a register within said block.

17. (Canceled)

18. (Currently Amended) A system according to Claim 31 ~~20~~, wherein said control register is operable to specify a plurality of ports.

19. (Cancelled)

20. (Currently Amended) ~~A system for expanding the addressing capability of a plurality of registers, the system comprising:~~

~~a plurality of blocks of registers, each block of registers having at least two registers;~~

~~a location register separate from the plurality of blocks of registers for selectively characterizing at least one of the blocks of registers as a specified block of registers,~~ A system according to Claim 31 wherein said location register includes a pointer to a plurality of location registers, each indicating a register block~~;~~

~~a control register separate from the plurality of blocks of registers for selecting at least one operational code for the specified block of registers and specifying at least one port number for the specified block of registers,~~ and wherein said control register includes a pointer to a plurality of control registers, each of the plurality of control registers storing a respective operational code, and wherein said plurality of location registers are associated with said plurality of control registers such that a first operational code is associated with a first block and a second operational code is associated with a second block~~; and~~

~~a control engine operable to access at least one of the first and second operational codes for the specified block of registers and act on the specified block of registers at each of the specified port numbers in accordance with the accessed operational code~~.

21. (Currently Amended) A system according to Claim 31 ~~20~~, wherein said operational codes each encode an operation selected from the group of operations consisting of pointer handling and stream looping.

22. (Currently Amended) A system according to Claim 31 ~~20~~, wherein said location and control registers are registers specified by IEEE standard 802.3 clause 22.

23-24. (Canceled)

25. (Currently Amended) A system according to Claim 31 ~~20~~ further comprising:

a mask register following the location register and specifying a mask for the specified block of registers.

26. (Currently Amended) A method for expanding addressing capability of a plurality of registers, comprising:

designating at least two of the plurality of registers as a block of registers;

providing a plurality of such blocks of registers;

designating a first register within the plurality of registers that is separate from the blocks of registers for selectively characterizing at least one of such blocks of registers as an indicated block of registers, such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer, the first register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification, the first register including a pointer to a plurality of location registers that each indicates at least one of the blocks of registers;

designating a second register within the plurality of registers that is separate from the blocks of registers for specifying at least one operation for the indicated block of registers, the second register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification, the second register including a pointer to a plurality of control registers in which each control register includes an operational code; and

associating said plurality of location registers with said plurality of control registers such

that a first operational code is associated with a first of such blocks of registers and a second operation code is associated with a second of such blocks of registers.

27. (Previously Presented) A method according to Claim 26, wherein the first register further comprises a block selector for selectively characterizing at least one of such blocks of registers as an indicated block of registers.

28. (Previously Presented) A method according to Claim 26, wherein the second register further comprises a port indicator.

29. (Previously Presented) A method according to Claim 26, wherein said location and control registers comprise registers compatible with IEEE standard 802.3 clause 22.

30. (New) A method for expanding addressing capability of a plurality of registers connected to an interface comprising:

designating at least two of the plurality of registers as a block of registers;

providing a plurality of such blocks of registers;

designating a first register within the plurality of registers that is separate from the blocks of registers for selectively characterizing at least one of such blocks of registers as an indicated block of registers such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer, the first register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification; and

designating a second register within the plurality of registers that is separate from the blocks of registers for specifying at least one operation for the indicated block of registers, the second register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification.

31. (New) A system for expanding the addressing capability of a plurality of registers, the system comprising:

a plurality of blocks of registers, each block of registers having at least two registers;

a location register separate from the plurality of blocks of registers for selectively characterizing at least one of the blocks of registers as a specified block of registers such that any of the registers of the indicated block of registers may be addressed without adjusting a pointer, the location register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification;

a control register separate from the plurality of blocks of registers for selecting at least one operational code for the specified block of registers and specifying at least one port number for the specified block of registers, the control register being compatible with IEEE standard 802.3 clause 22 and designated by the standard as available for vendor specification; and

a control engine operable to access the operational code for the specified block of registers and act on the specified block of registers at each of the specified port numbers in accordance with the operational code.

32. (New) A system according to Claim 31, wherein said location register includes a pointer to a plurality of location registers, each of the plurality of location registers including a block selector.

33. (New) A system according to Claim 31, wherein said control register is operable to store an operational code.

34. (New) A system according to Claim 33, wherein said control register is further operable to store a port indicator.

35. (New) A system according to Claim 31, wherein said control register includes a pointer to a plurality of control registers, each having an operational code.